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PROVISIONAL APPLICATION

Michelle Denise Griglione

Case: **5**

Title: **Creation of A High Ge Concentration SiGe Layer In BiCMOS Processing Through Thermal Oxidation of the SiGe Base Layer**

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Date: 3-11-04

Creation of a High Ge Concentration SiGe Layer In Bipolar or BiCMOS Processing Through Thermal Oxidation Of The SiGe Base Layer

In the past, methods for formation of an epitaxially grown layer of SiGe on a Si layer have resulted in layers of SiGe having limited concentrations of Ge. Generally, as the Ge content increases, the compressive strain in the SiGe layer also increases. Undesirable dislocations form in order to relieve strain formed in the SiGe layer. My invention allows a much higher Ge concentration to be achieved in the base regions of SiGe bipolar transistors while minimizing or eliminating lattice defects.

According to the prior methods, epitaxial growth of an as-deposited SiGe base layer film (formed on a Si layer) can have a somewhat elevated Ge concentration, on the order of about 30 percent, through careful control of the temperature, pressure and reactive gas flow rate during growth, and/or selection of a buffer layer between the Si and SiGe layers. Even with careful control of the growth conditions, as well as use of a buffer layer, dislocations within the high-Ge-concentration SiGe layer occur and this has limited the maximum Ge concentration achievable in the layer.

According to the invention, thermal oxidation of a SiGe layer in a bipolar device can result in a defect-free SiGe sublayer along the SiGe/oxide interface, characterized by a high Ge concentration relative to the as-deposited Ge concentration in other portions of the SiGe layer.

Oxidation of a SiGe layer will result in concentration of Ge atoms at the SiGe/oxide interface. It is believed that, during the oxidation process, Ge in the oxidizing region diffuses or otherwise migrates to form a sublayer of SiGe having a relatively high concentration of Ge. After oxidation there is a high Ge-concentration lattice region forming a sublayer of the SiGe layer along the interface of the oxide and the lattice structure. This high Ge concentration sublayer is referred to as a Ge pile-up region. When formed according to the invention the Ge pile-up region has crystalline properties similar, or equivalent, to an epitaxially grown layer and can be nearly or completely defect-free, despite the presence of a high Ge concentration. This invention employs oxidation in bipolar processing to achieve high Ge concentrations in epitaxially grown SiGe base layers. The range of Ge concentration in the low-defect Ge pile-up region can have an upper value of five times or more the original Ge concentration in the as-grown layer.

In a fabrication sequence according to the invention, a graded SiGe base is epitaxially grown on a Si collector layer as is common in standard SiGe BiCMOS processing (See Fig. 1). Typically, a crystalline or polycrystalline Si emitter layer is then epitaxially grown or otherwise deposited on top of the SiGe base. However, in order to form a low-defect density Ge pile-up region along an upper surface of the SiGe base, the SiGe base layer is thermally oxidized before the emitter layer is grown/deposited. (See Fig. 2) It should also be noted that the as-deposited SiGe base layer can have either graded dopant profile or a uniform Ge concentration throughout. A graded profile (with an increased Ge concentration near the upper surface) may facilitate creating an optimum Ge concentration in the Ge pile-up region.

Dry or wet oxidation can be employed to form an oxide layer (predominately a silicon oxide) from the upper portion of the SiGe base layer. Preferably, the oxidation temperature will vary from approximately 700 to 900 °C. Oxidation in this application may be performed at atmospheric pressure. A dry oxidation can be performed at gas flow rates of approximately 2 liters/min. The time duration of oxidation can vary, as this parameter determines the thickness and composition of the Ge pile-up area. In this invention, after oxidation of the SiGe layer, the thermal oxide is removed/stripped using a standard HF etch (See Fig 3), and

the Si emitter layer is then grown/deposited. (See Fig. 4) An exemplary oxidation includes dry oxidation at 900 °C for 1 hour at atmospheric pressure and O_2 flow rate of 2 liters/min.

During thermal oxidation of the SiGe layer, SiO2 (not necessarily stoichiometric) is preferentially produced compared to GeO2. The resulting oxide is therefore almost entirely silicon oxide. It is believed that the unbound Ge accumulates into a reformed lattice region below the oxide interface, creating a SiGe alloy region with high Ge content (i.e., the Ge pile-up region). See Fig. 2. When the base is formed with a graded SiGe layer, i.e., with a relatively high concentration near the surface (for example, 25 percent or more Ge) - as opposed to a uniform concentration of Ge throughout the SiGe layer, a low-defect density single crystal lattice can still be achieved in the Ge pile-up region, and the desirable compressive strain properties of the SiGe will remain. The final result is a defect-free or nearly defect-free SiGe region below the silicon oxide layer wherein the SiGe region is much higher in Ge concentration than achievable by standard epitaxial methods. Removal of the oxide layer from the surface using standard CMOS processing techniques exposes the high concentration SiGe base layer in preparation for emitter deposition/growth. See Fig. 3.

This method can also apply to other microelectronic devices that need low-defect level, high-Ge concentration SiGe layers.

Secondary Ion Mass Spectroscopy can be performed to quantify the concentration of Ge as well as the thickness of the final SiGe layer. TEM can confirm the thickness and crystalline quality of the SiGe layer. Final electrical performance of the bipolar device will reveal improvements attributable to the higher Ge concentration SiGe layer.

The following publications provide information relevant to characteristics and processing of materials in relation to Ge pile up regions and are incorporated herein by reference:

"Dry Thermal Oxidation Of A Graded SiGe Layer", Applied Physics Letters, Volume 79, Number 22, Pgs 3606- 3608, November 26, 2001

"Oxidation Study of SiGe", Journal of Applied Physics, Volume 65, Number 4, Pgs. 1724-1728, February 1989.

I claim:

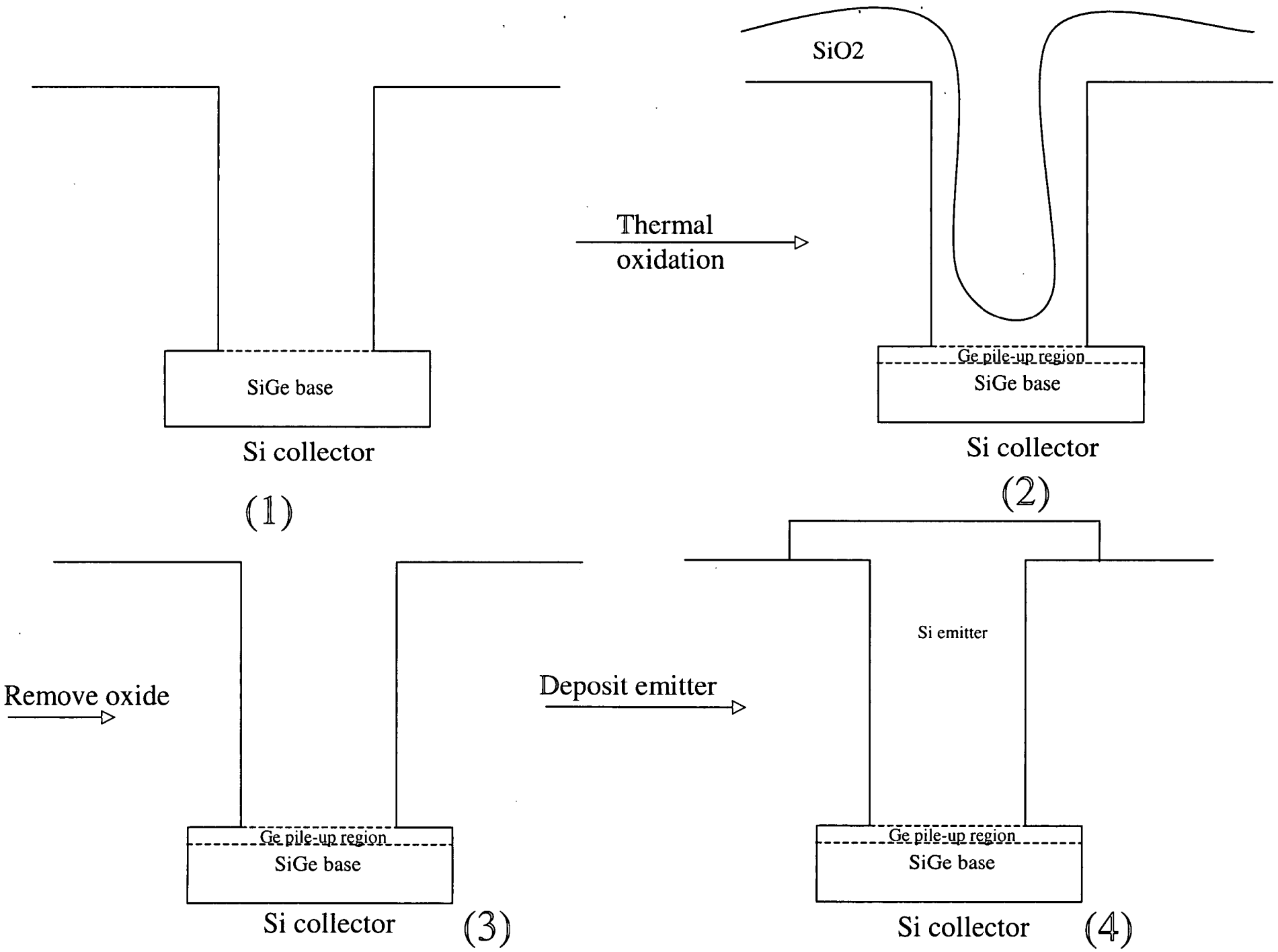
A method of manufacturing a semiconductor device comprising:

forming a SiGe base region, having a first upper surface, over a collector region;

reacting the base region along the upper surface to form a thermally grown oxide in the first upper surface;

removing the thermally grown oxide to expose a second upper surface of the base region; and

forming an emitter region over the base region.


SiO2
Thermal
oxidation
SiGe base
Si collector
(1)
Ge pile-up region
SiGe base
Si collector
(2)
Remove oxide
Deposit emitter
Si emitter
Ge pile-up region
SiGe base
Si collector
(3)
Ge pile-up region
SiGe base
Si collector
(4)